management system, programmable registers which set priorities for each processor, instructions, or instruction operands.

23. A multiple priority non-blocking load buffer according to Claim 15, wherein a maximum number of outstanding I/O transactions is specified for said unique priority level in each of said sub-queues which prevents entries of memory or I/O requests having low priority levels from using one of said sub-queues before entries of memory or I/O requests having higher priority levels.

24. A multiple priority non-blocking load buffer according to Claim 10, wherein priorities corresponding to entries of I/O requests are determined by logical memory addresses, control bits derived from a memory management page table, control bits derived from segmentation entries, virtual addresses of a memory management system, programmable registers which set priorities for each processor, instructions, or instruction operands.

25. A method according to Claim 18, further comprising the step of specifying a maximum number of outstanding memory or I/O transactions for said unique priority levels in each of said queues which prevents entries of memory or I/O transactions having low priority levels from using one of said queues before entries of memory or I/O transactions having higher priority levels.

26. A method according to Claim 18, further comprising the step of determining priorities corresponding to entries of memory or I/O transactions by logical memory addresses, control bits derived from a memory management page table, control bits derived from segmentation entries, virtual addresses of a memory management system, programmable registers which set priorities for each processor, instructions, or instruction operands.--